VEGA AS1061 – 64-bit Single Core Microprocessor

1. Device Overview

1.1. Features

- RISC-V 64G (RV64IMAFD) ISA
- 6 stage in-order pipeline implementation
- Advanced branch predictor: BTB, BHT, RAS
- Harvard architecture
- Privilege Levels : Supervisor and Machine-mode
- Configurable L1 caches
- High-performance IEEE 754-2008 compliant floating-point unit
- AXI4 or AHB compliant external interface
- Vectored interrupt support

- Platform Level Interrupt Controller
  - Up to 127 IRQs
  - Low interrupt latency
- Advanced Integrated Debug Controller
  - JTAG compliant interface
  - HW/SW breakpoints support
- Debug extension allowing Eclipse debugging via a GDB >> openOCD >> JTAG connection
- Linux compatible
- Zephyr compatible
- FreeRTOS port

1.2. Applications

- Consumer Electronics
- Motor Control
- Industrial Automation
- Wearable devices
- Motor drives
- Hand held devices
- GPS platforms

- Toys
- Electronic education devices
- PLCs
- Inverters
- Printers & Scanners
- Industrial networking
- Legacy 8/16-bit applications

1.3. Description

VEGA AS1061 features an in-order processing engine with a 6 stage pipeline enabling it to meet high-performance embedded application requirements. The processor also supports single and double precision floating point instructions, and MMU for Linux based applications. AS1061 is optimized for high performance with integrated Instruction Cache, Data Cache and an advanced branch predictor enabling efficient branch execution. Features also include PLIC and vectored interrupts for serving various types of system events. An AXI or AHB interface enables ease of system integration and JTAG debug interface for development support.
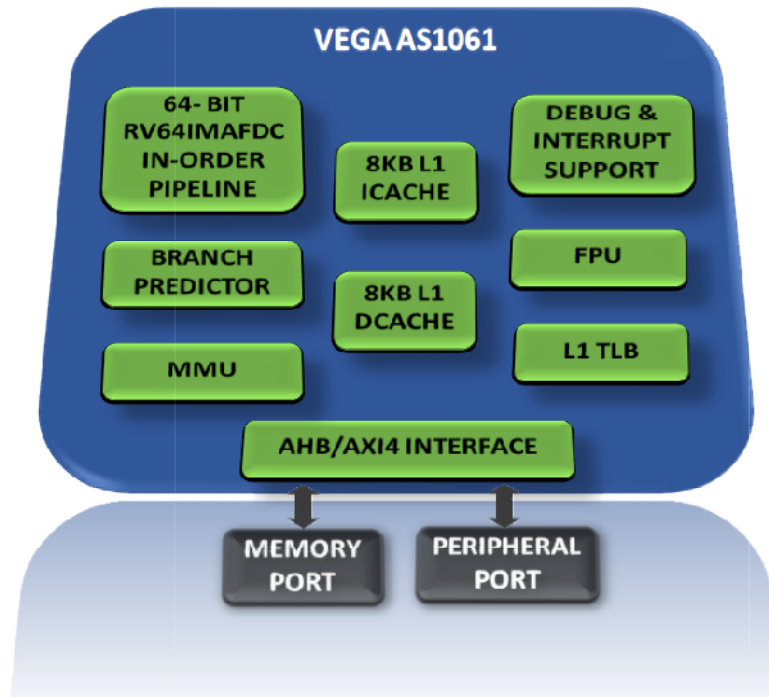
Figure 1: VEGA AS1061 Block Diagram

1.4. Deliverables

- RTL Source Code
- Test Benches
- Synthesis Scripts

- Product Specification
- User Guide
- Integration Guidelines

2. References

2.1. Website

https://vegaprocessors.in/

2.2. YouTube

https://www.youtube.com/VEGAProcessors

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PAGE 2